Inverter-Based Low-Voltage CCII- Design and Its Filter Application

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Abstract. *This paper presents a negative type second-generation current conveyor (CCII-). It is based on an inverter-based low-voltage error amplifier, and a negative current mirror. The CCII- could be operated in a very low supply voltage such as ±0.5 V. The proposed CCII- has wide input voltage range (±0.24 V), wide output voltage (±0.24 V) and wide output current range (±24 mA). The proposed CCII- has no on-chip capacitors, so it can be designed with standard CMOS digital processes. Moreover, the architecture of the proposed circuit without cascoded MOSFET transistors is easily designed and suitable for low-voltage operation. The proposed CCII- has been fabricated in TSMC 0.18μm CMOS processes and it occupies 1189.91×1178.43μm^2 (include PADs). It can also be validated by low voltage CCII filters.*

Keywords

Negative type second generation current conveyor, inverter-based low-voltage error amplifier, negative current mirror.

1. Introduction

In a hand held system and biomedical implant system, the main power supply is a battery, so the mobile control analog integrated circuit needs to match small volume, low-voltage, low-power, and high output voltage and current characteristics to improve the battery life [1], [2]. In analog circuit design, current-mode circuits have many well-known advantages. For example, they provide high-performance in speed, bandwidth and precision, yet consume less power [3], [4]; thus, they have found wide applications in high-performance active circuits. Current-mode circuits do not need high voltage gain nor high precision passive components. They can be applied in all transistor designs, which make them compatible with typical digital processes [5].

Since Smith and Sedra released the second generation current conveyor in 1970, it has served as the basic current-mode circuits [6]. Since then, the CCII has been used in many application circuits. The portability and the low-power consumption has enabled them to be widely used in battery-powered products, such as hearing aids [7-9], implantable cardiac pacemakers [10], mobile phone [11] and hand held multimedia terminals [12].

The second-generation current conveyor, CCII, is a popular current-mode circuit [13-17]. Most of the two supply voltage current conveyors require ±0.75 V supply voltage or higher, but their output currents are less than 1 mA [18], [19]. These current conveyors are designed with a class AB cascoded current mirror. The cascoded current mirror is not a very low-voltage structure. Recently, there are some papers that proposed a low supply-voltage (less than or equal to ±0.5 V) CCII, and their theory was simulated in HSPICE but was not fabricated and validated into an integrated circuit [20], [21]. These current conveyors are based on quasi-floating gate transistors, which are based on float-gate transistors. Therefore, they are not suitable for low-frequency filter and oscillator applications, and cannot be fabricated with standard CMOS digital processes. Moreover, the linear capacitors will cause a larger chip area. They will increase the cost of chip fabrication.

This paper proposes current-mode active components based on a inverter-based low-voltage error amplifier [22], [23] and a negative current mirror [24] – the negative second-generation current conveyor (CCII-). This new component uses an inverter-based low-voltage error amplifier instead of class AB amplifier or other amplifier in the conventional CCII. To compare with conventional CCII, this inverter-based low-voltage error amplifier based CCII- has low supply voltages, wide input voltages, and wide output voltages and currents. They can be operated at very low supply voltage (±0.5 V). Their input voltage ranges from ±5 $\mu V_{p\text{-}p}$ to ±240 $mV_{p\text{-}p}$, which will output the same voltage and generate ±0.5 $\mu A_{p\text{-}p}$ to ±24 $mA_{p\text{-}p}$ current with 10 Ω output load. Thus, they are highly compatible with various types of analog circuits.

Analog engineers have used current conveyor extensively to design circuits such as filters [25], oscillators [26], rectifiers [27], and low-noise amplifiers [28]. In recent years, active filters are more important in power electronics and analog signal processing. Because of the development of current mode circuits, the performance of analog circuits has improved considerably. The active filters of a current conveyor have since received more attention in biquad filter design [29], [30].

This research focuses on CMOS processes. It uses a CMOS characteristic and an inverter-based low-voltage error amplifier as well as a negative current mirror to construct a new CCII-. We designed a chip of negative second generation current conveyor (CCII-) for fabrication.

2. Circuit Description

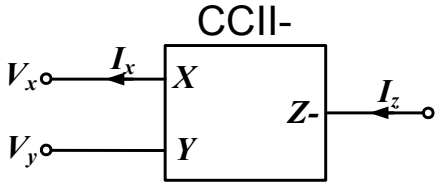

Fig. 1. Negative current conveyor (CCII-).

CCII- is a three-terminal element as shown in Fig. 1. The ideal CCII characteristic equation can be described in (1). *Y* terminal having a high input impedance, can be used as a voltage mode input terminal used to input voltage signal. The *Y* terminal has no current flows ($I_y = 0$), but it transmits the same voltage signal to the X terminal ($V_x = V_y$). *X* terminal has low input impedance, so it can output voltage and current. When the X terminal is connected to a load, a current flows into the X-side, and the current is reversed and transmitted to the *Z*- terminal ($I_z = -I_x$). Z- terminal has high output impedance, suitable for working in the current mode.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1}$$

Fig. 2 is a complete circuit diagram of the proposed inverter-based low-voltage current conveyor. This inverter-based low voltage error amplifier [22], [23], shown in the leftmost portion of Fig. 2, is a 2-input and 2-output low-voltage error amplifier. The output of the inverter-based low-voltage error amplifier via the differential to single amplifier, shown in the middle portion of Fig. 2, turn into a single-ended output. These two parts use closed-loop

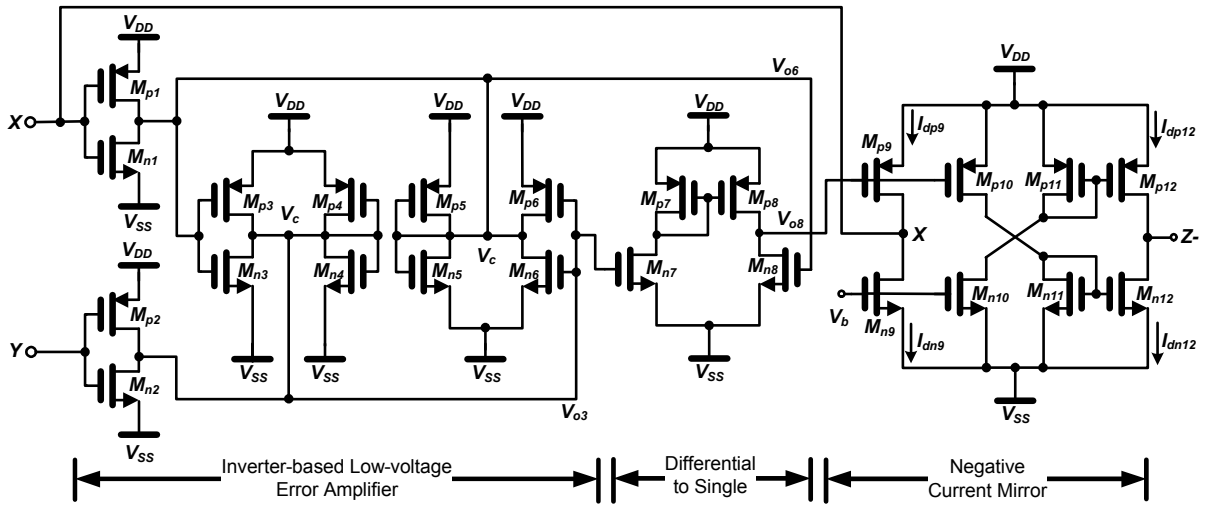

Fig. 2. The inverter-based low-voltage CCII- circuit.

negative feedback mechanism to stabilize the voltage. In the rightmost portion of Fig. 2, the negative current mirror copies and reverses *X* terminal current to *Z* terminal. The above three parts are connected together to form a negative current conveyor.

The proposed inverter-based low-voltage CCII- circuit will be analyzed step by step as follow. First, we discuss the single inverter as shown in Fig. 3(a), which is the same as Inv_1, Inv_2, Inv_3 and Inv_6 in Fig. 2. Its output and input voltage relationships can be given as (2). Subsequently seen from Fig. 3(a), flowing through the NMOS current I_{dn} and the PMOS current I_{dp} are represented by (3) and (4). Thus, a single inverter output current I_{out} is represented by (5).

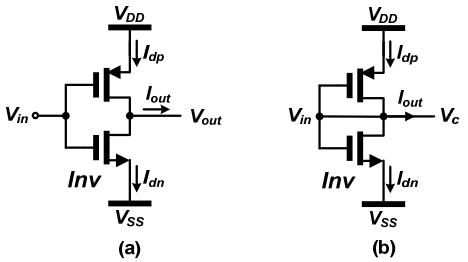

Fig. 3. (a) The single inverter (b). The single inverter with input voltage equal to output voltage.

$$A_{Vd} = \frac{g_{mn1,2} - g_{mp1,2}}{g_{mp1,2} + \dfrac{1}{r_{op1,2}} + \dfrac{1}{r_{on1,2}}}, \tag{2}$$

$$I_{dn} = \frac{\beta_n}{2}\left(V_{gsn} - V_{tn}\right)^2 = \frac{\beta_n}{2}\left(V_{in} - V_{SS} - V_{tn}\right)^2, \quad (3)$$

$$I_{dp} = \frac{\beta_p}{2}\left(V_{gsp} - V_{tp}\right)^2 = \frac{\beta_p}{2}\left(V_{in} - V_{DD} - V_{tp}\right)^2 \quad (4)$$

where $\beta_n = \frac{\mu_n C_{ox} W_n}{L_n}$, $\beta_p = \frac{\mu_p C_{ox} W_p}{L_p}$, and

$$I_{out} = I_{dp} - I_{dn}. \quad (5)$$

When the inverter input and output terminals are connected together as shown in Fig. 3(b), which is the same as Inv_4 and Inv_5 in Fig. 2. Therefore, the function of Inv_4 and Inv_5 in the circuit is equivalent to a resistor. Because $V_{in} = V_c$, then $I_{out} = 0$. When we substitute (3) and (4) into (5), V_c can then be expressed as (6). If $V_{ss} = -V_{dd}$ and $V_{tn} = -V_{tp}$, then V_c can be simplified as (7).

$$V_c = \frac{\left(V_{DD} + V_{tp}\right) - \sqrt{\frac{\beta_n}{\beta_p}}\left(V_{SS} + V_{tn}\right)}{\left(1 - \sqrt{\frac{\beta_n}{\beta_p}}\right)}, \quad (6)$$

$$V_c = \frac{\left(1 + \sqrt{\frac{\beta_n}{\beta_p}}\right)\left(V_{DD} + V_{tp}\right)}{\left(1 - \sqrt{\frac{\beta_n}{\beta_p}}\right)}. \quad (7)$$

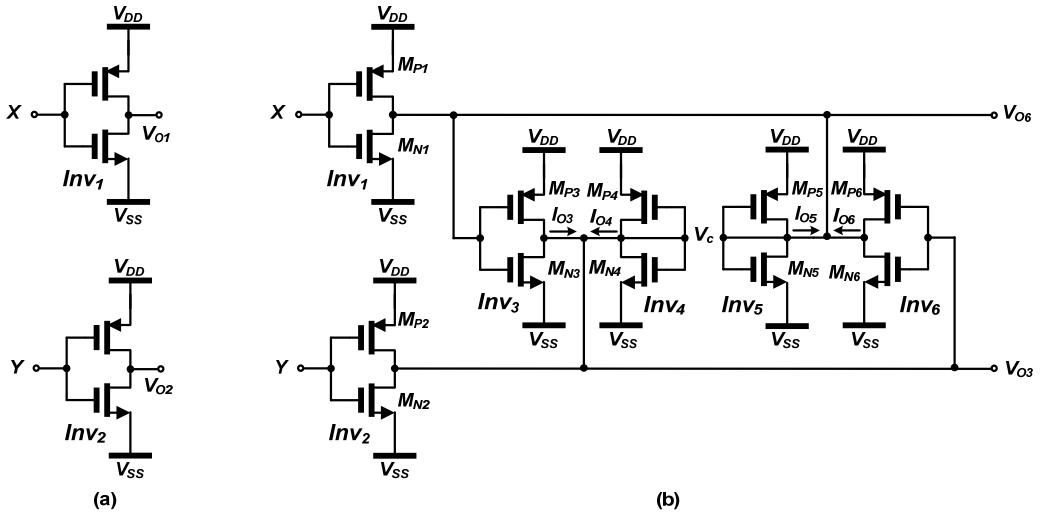

Fig. 4. (a) Two balanced inverters. (b) The inverter-based low-voltage error amplifier.

Fig. 4(a) shows the inverter Inv_1 and Inv_2. Fig. 4(b) shows the inverter-based low-voltage error amplifier circuit. From Fig. 4(a), X and Y terminal are the inputs of Inv_1 and Inv_2, respectively. The output voltage of Inv_1 and Inv_2 can be given as (8) and (9), respectively.

$$V_{o1} = -\frac{g_{mn1} - g_{mp1}}{g_{mp1} + \frac{1}{r_{op1}} + \frac{1}{r_{on1}}} V_x, \quad (8)$$

$$V_{o2} = -\frac{g_{mn2} - g_{mp2}}{g_{mp2} + \frac{1}{r_{op2}} + \frac{1}{r_{on2}}} V_y. \quad (9)$$

From Fig. 4(b), the input and output of Inv_4 and Inv_5 are connected together, which are equivalent to resistors. Inv_3 and Inv_6 are differential pairs, whose common mode voltage V_c shows as (7). The common-mode level of the output voltages V_{06} and V_{03} is controlled by the four inverters (Inv_3, Inv_4, Inv_5 and Inv_6) of Fig. 4(b). The values of these resistances are $1/gm_3$, $1/gm_4$, $1/gm_5$ and $1/gm_6$. Inv_3 and Inv_6 generate currents $gm_3(V_c\text{-}V_{01})$ and $gm_6(V_c\text{-}V_{02})$, respectively. Thus, V_{03} and V_{06} can be given as (10) and (11), respectively. The input voltage difference (V_{id}) of Inv_1 and Inv_2 can be obtained as (12). If $g_{mp1} = g_{mp2} = g_{mp1,2}$, $g_{mn1} = g_{mn2} = g_{mn1,2}$, $r_{op1} = r_{op2} = r_{op1,2}$, $r_{on1} = r_{on2} = r_{on1,2}$, their differential output voltage V_{od} is equal to $V_{06}\text{-}V_{03}$, and can be obtained by (13). Finally, the voltage gain of inverter-based low-voltage error amplifier A_{Vd} can be obtained as (14).

$$V_{o3} = \frac{I_{o3}}{g_{mp3}} = \left(V_c - V_{01}\right), \quad (10)$$

$$V_{o6} = \frac{I_{o6}}{g_{mp6}} = \left(V_c - V_{02}\right), \quad (11)$$

$$V_{id} = V_y - V_x, \quad (12)$$

$$V_{od} = V_{06} - V_{03} = V_{o1} - V_{o2} = \frac{g_{mn1,2} - g_{mp1,2}}{g_{mp1,2} + \frac{1}{r_{op1,2}} + \frac{1}{r_{on1,2}}}\left(V_y - V_x\right), \quad (13)$$

$$A_{Vd} = \frac{V_{od}}{V_{id}} = \frac{g_{mn1,2} - g_{mp1,2}}{g_{mp1,2} + \frac{1}{r_{op1,2}} + \frac{1}{r_{on1,2}}}. \quad (14)$$

Fig. 5 is a differential to single amplifier. It is also the intermediate portion of Fig. 2. The two output of inverter-based low-voltage error amplifier coupled to the two inputs of a differential to single amplifier. The differential to single amplifier turns into a single-ended output. Its output voltage and voltage gain can be given as (15) and (16).

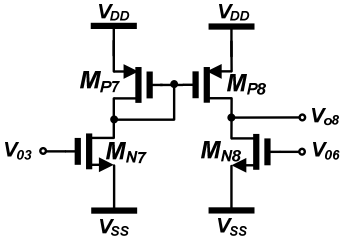

Fig. 5. The differential to single amplifier.

$$V_{o8} = g_{mp7}\left(r_{0p8} // r_{0n8}\right)\left(V_{06} - V_{03}\right), \quad (15)$$

$$A_{Vs} = \frac{V_{08}}{V_{06} - V_{03}} = g_{mp7}\left(r_{op8} // r_{on8}\right). \quad (16)$$

Last but not least, Fig. 6 shows the negative current mirror circuit, which is shown as the rightmost part of Fig. 2. The input of M_{p9} and M_{p10} is the output of differential to single amplifier, while the CS_9 output feedback to the CCII- X terminal to let $V_x = V_y$. The CS_9 and CS_{10} are the positive current mirror and if another current mirror CS_{11} and CS_{12} is added, but the output of CS_{10} is broken and cross connected to the inputs of CS_{11} to invert the current polarity and form a negative current mirror. For example, the drain of M_{p10} is connected to the drain of M_{n11} and the drain of M_{n10} is connected to the drain of M_{p11}, so $I_z = -I_x$.

From Fig. 6, the input resistor R_{i9} can be given as (17) and the output resistor R_{o9} can be given as (18). Thus, the output voltage V_x can be represented as (19) and the voltage gain of common source stage (A_{Vx}) can be obtained as (20).

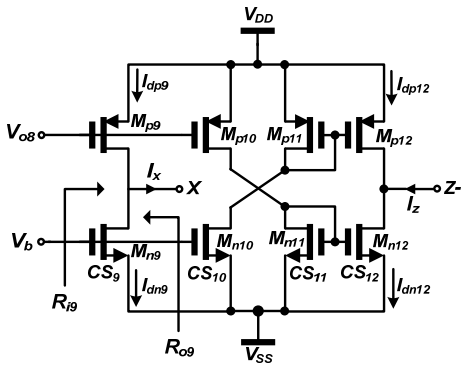

Fig. 6. Negative current mirror.

$$R_{i9} = \infty, \quad (17)$$

$$R_{o9} = \frac{r_{on9} // r_{op9}}{1 + A_{Vtotal}}, \quad (18)$$

$$V_x = \left(g_{mp9} R_{o9}\right) \times V_{08}, \quad (19)$$

$$A_{Vx} = \frac{V_x}{V_{08}} = g_{mp9} R_{o9}. \quad (20)$$

Finally, we composed the above three parts, low-voltage error amplifier, differential to single amplifier and negative current mirror, to form a low-voltage CCII-. The total voltage gain of this composed CCII- can be obtained as (21). The voltage gain of each part depends on the transistor's g_m and r_o. Hence, adjusting the W/L of transistors, will make $A_{Vd} \times A_{Vs} \times A_{Vx} >> 1$, $A_{Vtotal} \approx 1$ and $V_x \approx V_y$.

$$A_{Vtotal} = \frac{V_x}{V_y} = \frac{A_{Vd} \times A_{Vs} \times A_{Vx}}{1 + \left(A_{Vd} \times A_{Vs} \times A_{Vx}\right)}. \quad (21)$$

For CCII-, the output current of terminal X and terminal Z can be given as (22) and (23) respectively. From Fig. 6, we know that $I_{dp9} = I_{dn12}$ and $I_{dn9} = I_{dp12}$. Thus, we obtain $I_z = -I_x$ or $I_{z-} = I_x$ and obtain A_I or A_{I-} as (24) or (25).

$$I_x = I_{dp9} - I_{dn9}, \quad (22)$$

$$I_{z-} = I_{dn12} - I_{dp12}, \quad (23)$$

$$A_I = \frac{I_z}{I_x} = \frac{I_{dp12} - I_{dn12}}{I_{dp9} - I_{dn9}} = -1, \quad (24)$$

$$A_{I-} = \frac{I_{z-}}{I_x} = \frac{I_{dn12} - I_{dp12}}{I_{dp9} - I_{dn9}} = 1. \quad (25)$$

3. Applications

To prove the functionality of this proposed CCII-, we implement a CCII- filter. Fig. 7 shows single CCII- based biquad filter [29]. The filter of Fig. 7 could be a low pass filter (V_1) and band pass filter (V_z).

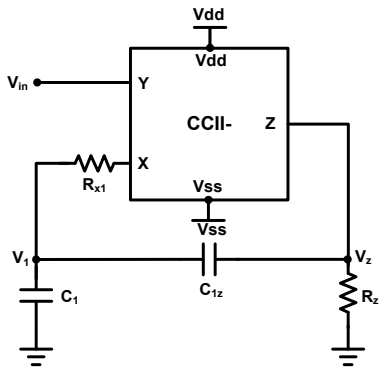

Fig. 7. The single CCII- biquad low-pass filters.

The characteristic equation of Fig. 7 is shown as (26). ω_0, Q and gain are given as (27), (28) and (29), respectively.

$$\frac{V_1}{V_y} = \frac{\dfrac{1}{R_{x1}R_z}}{s^2 C_1 C_{1z} + s\left(C_1 + C_{1z}\right)\dfrac{1}{R_z} + \dfrac{1}{R_{x1}R_z}}, \tag{26}$$

$$\omega_0 = \sqrt{\frac{1}{C_1 C_{1z} R_{x1} R_z}}, \tag{27}$$

$$Q = \sqrt{\frac{1}{C_1 + C_{1z}}\left(\frac{R_z}{R_{x1}} C_1 C_{1z}\right)}, \tag{28}$$

$$\text{and gain} = -1. \tag{29}$$

4. Experimental Results

Fig. 8 shows the micro photograph of the proposed CCII-. The chip area of CCII- is 1189.91×1178.43 μm^2, which is fabricated with TSMC 0.18 μm CMOS processes. The aspect ratios of MOS transistors are shown in Tab. 1.

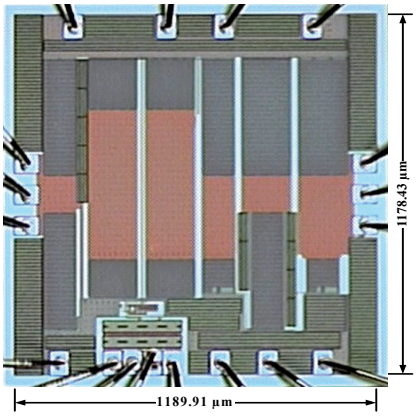

Fig. 8. Chip photographs of the proposed CCII-.

Transistor	W/L(μm)	Transistor	W/L(μm)
M_{p1}, M_{p2}	1/1	M_{n1}, M_{n2}	1/1
M_{p3}, M_{p4}	4/1	M_{n3}, M_{n4}	1/1
M_{p5}, M_{p6}	4/1	M_{n5}, M_{n6}	1/1
M_{p7}, M_{p8}	3/1	M_{n7}, M_{n8}	1/1
M_{p9}, M_{p10}	10/1	M_{n9}, M_{n10}	10/1
M_{p11}, M_{p12}	10/1	M_{n11}, M_{n12}	10/1

Tab. 1. Aspect ratios of MOS transistors in proposed CCII-.

4.1 CCII Experimental Results

The proposed chips can be operated at ±0.5 V supply voltages. The performances of the proposed CCII- are listed in Tab. 2. At ±0.5 V supply voltages, Tab. 2 shows the input, output voltages/currents and other parameters, such as the voltage tracking error and 3dB voltage bandwidth from Y to X, and the current tracking error and 3dB current bandwidth from X to Z, and parasitic parameters R_y, C_y, R_x, L_x, R_z, C_z, and power consumption.

	Parameter	CCII-
Inputs	V_{DD}	+0.50 V
	V_{SS}	-0.50 V
	V_b	+0.072 V
	V_y	±0.24 Vp-p
Outputs	V_x	±0.24 Vp-p
	I_x	±24 mAp-p
	I_z	∓ 24 mAp-p
function	*Voltage tracking error*	0.01 %
	Vy/Vx bandwidth	36.0 MHz
	Voltage performance	99.99 %
	Current tracking error	0.15 %
	Iz/Ix bandwidth	30.2 MHz
other	R_y	1.4 GΩ
	C_y	2.75×10^{-18} F
	R_x	137 KΩ
	L_x	5.28×10^{-4} H
	R_z	225 KΩ
	C_z	6.2×10^{-15} F
	Power Consumption	120 mW

Tab. 2. The performances of the proposed CCII-

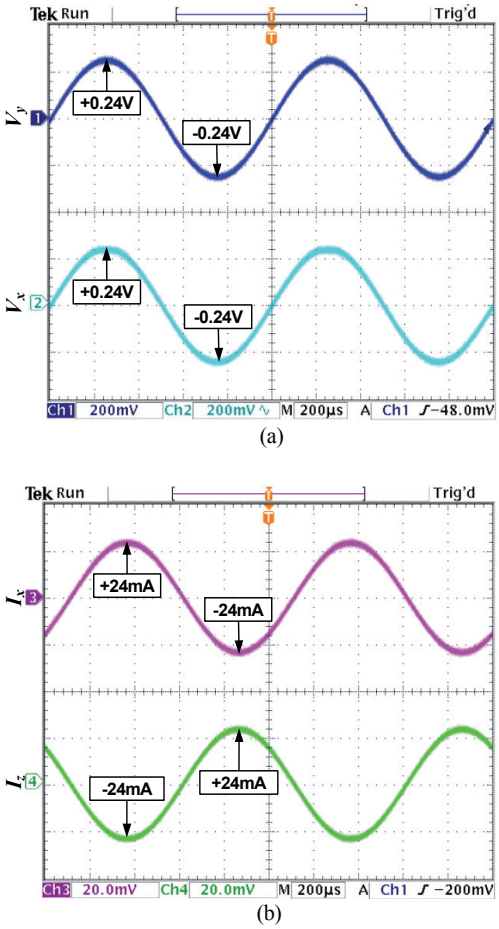

Fig. 9. The experimental waveforms of the proposed CCII- at Vsupply = ±0.5 V, (a) Vy & Vx , (b) Ix & Iz.

Because the output current is proportional to the power consumption and the proposed CCII- is designed for high output current, hence the power consumption is high. If the dimensions of Mp7~Mp12 and Mn7~Mn12 are divided by 10 and the input voltage (V_y) is also divided by 10, then the output current (I_x, I_z) and power consumption

are reduced to one tenth. Similarly, if the dimensions of Mp7~Mp12 and Mn7~Mn12 are divided by 100 and the input voltage (V_y) is also divided by 100, then the output current (I_x, I_z) and power consumption are reduced to one percent.

Fig. 9 shows the experimental waveforms of the proposed CCII- operating at ±0.5 V supply voltages. Fig. 9(a) shows the input voltage waveforms of terminal *Y* and output voltage waveforms of terminal *X*. Fig. 9(b) shows the output current waveform of terminal *X* and duplicate reversed current waveform of terminal *Z*-.

From the experimental waveforms, the proposed CCII- functionalities are good. The input voltage of terminal Y of the proposed CCII- can be raised to ±0.24 V with ±0.5 V supply voltages and it will generate the same output voltage at terminal X, which is 48% of the supply voltage. Terminal X and Z- of CCII- generate ±24 mA and ∓24 mA currents, respectively. Those output voltages and currents are almost 10 times the voltage and current of other CCII [18-21] designs.

4.2 Filter Experimental Result

To validate the functionality of this proposed CCII-, we implement a CCII- biquad filter using Fig. 7 circuit. The frequency response of the proposed CCII- LPF (Fig. 7) was validated with ±0.5 V supply voltages, +0.08 V bias voltage and the passive components $R_{x1} = 2$ kΩ, $C_1 =$ 100 pF, $C_{1z} = 100$ pF, $R_z = 1.5$ KΩ. The experimental waveforms of the proposed CCII- LPF are shown in Fig. 10.

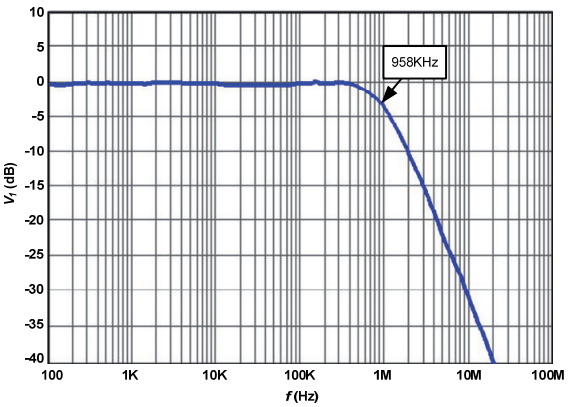

Fig. 10. The magnitude and bandwidth of this proposed CCII- LPF with ±0.5 V supply voltage

V_{supply}(V)	V_b(V)	R_{x1}(KΩ)	R_z(KΩ)	$C_1 = C_{1z}$(F)	BW(Hz)
±0.5V	+0.08	2.0	1.5	100n	960
±0.5V	+0.08	2.0	1.5	10n	9.56K
±0.5V	+0.08	2.0	1.5	1n	97.0K
±0.5V	+0.08	2.0	1.5	100p	958K
±0.5V	+0.08	2.0	1.5	10p	9.60M
±0.5V	+0.08	2.0	1.5	1p	33.0M
±0.5V	+0.08	2.0	1.5	0.1p	35.8M

Tab. 3. Experimental results of this proposed CCII- biquad filter operating at ±0.5 V supply voltage and +0.08 V bias voltage.

By changing C_1 and C_{1z}, the bandwidths of the proposed CCII- LPF are listed in Tab. 3.

Finally, we compare the proposed current conveyor with previous works in [18], [20] and list the results in Tab. 4.

Parameter	This CCII-	CCII in [18]	CCII in [20]
CMOS technology	0.18 μm	0.35 μm	0.35 μm
Experimental results	Measured results	Simulation results	Simulation results
Fabricated	Yes	No	No
Suitable for standard CMOS digital processes	Yes	Yes	No
Supply voltage	±0.5V	±0.75V	±0.5V
Number of linear capacitors	0	0	4
Low-voltage architecture	Yes	No	Yes
Current driving capability	±24 mA	±4 mA	±0.3 mA

Tab. 4. Comparison of the proposed current conveyor and previous works.

5. Conclusion

New inverter-based low-voltage CCII- is presented. In the proposed CCII-, there are no linear capacitors and they can be designed with standard CMOS digital processes that will reduce the cost of chip fabrication. The architecture of the proposed CCII- without cascoded MOSFET transistors is easily designed and suitable for low-voltage operation. This proposed CCII- can be operated in wide dynamic input range such as ±240 mV and low supply voltage such as ±0.5 V. It can work in wide input voltage ±0.24 V, and generate wide output voltage ±0.24 V and large output current ±24 mA. Its output voltages and currents are almost 10 times the voltage and current of other CCII designs. This proposed CCII- has been fabricated in TSMC 0.18μm CMOS processes and it occupies 1189.91×1178.43 μm^2 (include PADs). It also can be validated by low voltage CCII- filters.

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